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22415 MICROPROCESSOR MCQ

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1) Which is the microprocessor comprises:
   a. Register section
   b. One or more ALU
   c. Control unit
   d. All of these
2) What is the store by register?
   a. data
   b. operands
   c. memory
   d. None of these
3) Accumulator based microprocessor example are:
   a. Intel 8085
   b. Motorola 6809
   c. A and B
   d. None of these
4) A set of register which contain are:
   a. data
   b. memory addresses
   c. result
   d. all of these
5) There are primarily two types of register:
   a. general purpose register
   b. dedicated register
   c. A and B
   d. none of these
6) Name of typical dedicated register is:
   a. PC
   b. IR
   c. SP
   d. All of these
7) BCD stands for:
   a. Binary coded decimal
   b. Binary coded decoded

c. Both a & b
d. none of these

8) Which is used to store critical pieces of data during subroutines and interrupts:
a. Stack
b. Queue
c. Accumulator
d. Data register

9) The data in the stack is called:
a. Pushing data
b. Pushed
c. Pulling
d. None of these

10) The external system bus architecture is created using from _____ architecture:
a. Pascal
b. Dennis Ritchie
c. Charles Babbage
d. Von Neumann

11) The processor 80386/80486 and the Pentium processor uses _____ bits address bus: a. 16
b. 32
c. 36
d. 64

12) Which is not the control bus signal:
a. READ
b. WRITE
c. RESET
d. None of these

13) PROM stands for:
a. Programmable read-only memory
b. Programmable read write memory
c. Programmer read and write memory
d. None of these

14) EPROM stands for:
a. Erasable Programmable read-only memory
b. Electrically Programmable read write memory
c. Electrically Programmable read-only memory
d. None of these

15) Each memory location has:
a. Address
b. Contents
c. Both A and B
d. None of these

16) Which is the type of microcomputer memory: a. Processor memory

b. Primary memory
c. Secondary memory
d. All of these

17) Secondary memory can store____:
a. Program store code
b. Compiler
c. Operating system
d. All of these

18) Secondary memory is also called____:
a. Auxiliary
b. Backup store
c. Both A and B
d. None of these

19) Customized ROMS are called:
a. Mask ROM
b. Flash ROM
c. EPROM
d. None of these

20) The RAM which is created using bipolar transistors is called: a. Dynamic RAM
b. Static RAM
c. Permanent RAM
d. DDR RAM

21) Which type of RAM needs regular referred:
a. Dynamic RAM
b. Static RAM
c. Permanent RAM
d. SD RAM

22) Which RAM is created using MOS transistors: **a. Dynamic RAM**
b. Static RAM
c. Permanent RAM
d. SD RAM

23) A microprocessor retries instructions from :
a. Control memory
b. Cache memory
c. Main memory
d. Virtual memory

24) The lower red curvy arrow show that CPU places the address extracted from the memory location on the_____:
a. Address bus
b. System bus
c. Control bus
d. Data bus

25) The CPU sends out a ____ signal to indicate that valid data is available on the data

bus: a. Read

b. Write

c. Both A and B

d. None of these

26) The CPU removes the ___ signal to complete the memory write operation: **a. Read**

b. Write

c. Both A and B

d. None of these

27) BIU STAND FOR:

a. Bus interface unit

b. Bess interface unit

c. A and B

d. None of these

28) EU STAND FOR:

a. Execution unit

b. Execute unit

c. Exchange unit

d. None of these

29) Which are the four categories of registers:

a. General- purpose register

b. Pointer or index registers

c. Segment registers

d. Other register

e. All of these

30) Eight of the register are known as:

a. General- purpose register

b. Pointer or index registers

c. Segment registers

d. Other register

31) The four index register can be used for:

a. Arithmetic operation

b. Multipulation operation

c. Subtraction operation

d. All of these

32) IP Stand for:

a. Instruction pointer

b. Instruction purpose

c. Instruction paints

d. None of these

33) CS Stand for:

a. Code segment

b. Coot segment

c. Cost segment

d. Counter segment

34) DS Stand for:

a. Data segment

b. Direct segment

c. Declare segment

d. Divide segment

35) Which are the segment:

a. CS: Code segment

b. DS: data segment

c. SS: Stack segment

d. ES:extra segment

e. All of these

36) The acculatator is 16 bit wide and is called: **a. AX**

b. AH

c. AL

d. DL

37) How many bits the instruction pointer is wide: **a. 16 bit**

b. 32 bit

c. 64 bit

d. 128 bit

38) How many type of addressing in memory: a. Logical address

b. Physical address

c. Both A and B

d. None of these

39) The size of each segment in 8086 is: **a. 64 kb**

b. 24 kb

c. 50 kb

d. 16kb

40) The _____ address of a memory is a 20 bit address for the 8086 microprocessor: **a. Physical**

b. Logical

c. Both

d. None of these

41) The pin configuration of 8086 is available in the_____:

a. 40 pin

b. 50 pin

c. 30 pin

d. 20 pin

42) DIP stand for:

a. Deal inline package

b. Dual inline package

c. Direct inline package

d. Digital inline package

43) EA stand for:
   a. Effective address
   b. Electrical address
   c. Effect address
   d. None of these

44) BP stand for:
   a. Bit pointer
   b. Base pointer
   c. Bus pointer
   d. Byte pointer

45) DI stand for:
   a. Destination index
   b. Defect index
   c. Definition index
   d. Delete index

46) SI stand for:
   a. Stand index
   b. Source index
   c. Segment index
   d. Simple index

47) ALE stand for:
   a. Address latch enable
   b. Address light enable
   c. Address lower enable
   d. Address last enable

48) NMI stand for:
   a. Non mask able interrupt
   b. Non mistake interrupt
   c. Both
   d. None of these

49) _____ is the most important segment and it contains the actual assembly language instruction to be executed by the microprocessor:
   a. Data segment
   b. Code segment
   c. Stack segment
   d. Extra segment

50) The offset of a particular segment varies from _____:
   a. 000H to FFFH
   b. 0000H to FFFFH
   c. 00H to FFH
   d. 00000H to FFFFFH

51) Which are the factor of cache memory:
   a. Architecture of the microprocessor

b. Properties of the programs being executed
c. Size organization of the cache
d. All of these

52) _____ is usually the first level of memory access by the microprocessor: **a. Cache memory**
b. Data memory
c. Main memory
d. All of these

53) Which is the small amount of high- speed memory used to work directly with the microprocessor:
a. Cache
b. Case
c. Cost
d. Coos

54) The cache usually gets its data from the_____ whenever the instruction or data is required by the CPU:
a. Main memory
b. Case memory
c. Cache memory
d. All of these

55) Microprocessor reference that are available in the cache are called_____:
a. Cache hits
b. Cache line
c. Cache memory
d. All of these

56) Microprocessor reference that are not available in the cache are called_____:
a. Cache hits
b. Cache line
c. Cache misses
d. Cache memory

57) Which causes the microprocessor to immediately terminate its present activity:
a. RESET signal
b. INTERUPT signal
c. Both
d. None of these

58) Which is responsible for all the outside world communication by the microprocessor:

a. BIU
b. PIU
c. TIU
d. LIU

59) INTR: it implies the_____ signal:
a. INTRRUPT REQUEST
b. INTRRUPT RIGHT
c. INTRRUPT RONGH

d. INTRRUPT RESET

60) Which of the following are the two main components of the CPU?
a. Control Unit and Registers
b. Registers and Main Memory
c. Control unit and ALU
d. ALU and bus

61) Different components n the motherboard of a PC unit are linked together by sets of parallel electrical conducting lines. What are these lines called?
a. Conductors
b. Buses
c. Connectors
d. Consecutives

62) The language that the computer can understand and execute is called
a. Machine language
b. Application software
c. System program
d. All of the above

63) Which of the following is used as a primary storage device?
a. Magnetic drum
b. PROM
c. Floppy disk
d. All of these

64) Which of the following memories needs refresh?
a. SRAM
b. DRAM
c. ROM
d. All of above

65) The memory which is programmed at the time it is manufactured
a. PROM
b. RAM
c. PROM
d. EPROM

66) Which of the following memory medium is not used as main memory system?
a. Magnetic core
b. Semiconductor
c. Magnetic tape
d. Both a and b

67) Registers, which are partially visible to users and used to hold conditional, are known as
a. PC
b. Memory address registers
c. General purpose register
d. Flags

68) One of the main feature that distinguish microprocessors from micro-computers is
a. Words are usually larger in microprocessors
b. Words are shorter in microprocessors

c. Microprocessor does not contain I/O devices

d. Exactly the same as the machine cycle time

69) The first microprocessor built by the Intel Corporation was called

a. 8008

b. 8080

c. 4004

d. 8800

70) An integrated circuit is

a. A complicated circuit

b. An integrating device

c. Much costlier than a single transistor

d. Fabricated on a tiny silicon chip

71) Most important advantage of an IC is its

a. Easy replacement in case of circuit failure

b. Extremely high reliability

c. Reduced cost

d. Low powers consumption

72) Which of the following items are examples of storage devices?

a. Floppy / hard disks

b. CD-ROMs

c. Tape devices

d. All of the above

73) The Width of a processor's data path is measured in bits. Which of the following are common data paths?

a. 8 bits

b. 12 bits

c. 16 bits

d. 32 bits

74) Which is the type of memory for information that does not change on your computer?

a. RAM

b. ROM

c. ERAM

d. RW / RAM

75) What type of memory is not directly addressable by the CPU and requires special softw3are called EMS (expanded memory specification)?

a. Extended

b. Expanded

c. Base

d. Conventional

76) Before a disk can be used to store data. It must be…….

a. Formatted

b. Reformatted

c. Addressed

d. None of the above

77) Which company is the biggest player in the microprocessor industry?

a. Motorola
b. IBM
c. Intel
d. AMD

78) A typical personal computer used for business purposes would have… of RAM. a. 4 KB
b. 16 K
c. 64 K
d. 256 K

78) The word length of a computer is measured in
a. Bytes
b. Millimeters
c. Meters
d. Bits

79) What are the three decisions making operations performed by the ALU of a computer?
a. Grater than
b. Less than
c. Equal to
d. All of the above

80) Which part of the computer is used for calculating and comparing?
a. Disk unit
b. Control unit
c. ALU
d. Modem

81) Can you tell what passes into and out from the computer via its ports?
a. Data
b. Bytes
c. Graphics
d. Pictures

82) What is the responsibility of the logical unit in the CPU of a computer? a. To produce result
b. To compare numbers
c. To control flow of information
d. To do math's works

83) The secondary storage devices can only store data but they cannot perform
a. Arithmetic Operation
b. Logic operation
c. Fetch operations
d. Either of the above

84) Which of the following memories allows simultaneous read and write operations?
a. ROM
b. RAM
c. EPROM
d. None of above

85) Which of the following memories has the shortest access times?

a. Cache memory
b. Magnetic bubble memory
c. Magnetic core memory
d. RAM

86) A 32 bit microprocessor has the word length equal to
a. 2 byte
b. 32 byte
c. 4 byte
d. 8 byte

87) An error in computer data is called
a. Chip
b. Bug
c. CPU
d. Storage device

88) The silicon chips used for data processing are called
a. RAM chips
b. ROM chips
c. Micro processors
d. PROM chips

89) The metal disks, which are permanently housed in, sealed and contamination free containers are called
a. Hard disks
b. Floppy disk
c. Winchester disk
d. Flexible disk

90) A computer consists of
a. A central processing unit
b. A memory
c. Input and output unit
d. All of the above

91) The instructions for starting the computer are house on
a. Random access memory
b. CD-Rom
c. Read only memory chip
d. All of above

92) The ALU of a computer normally contains a number of high speed storage element called
a. Semiconductor memory
b. Registers
c. Hard disks
d. Magnetic disk

93) The first digital computer built with IC chips was known as
a. IBM 7090
b. Apple – 1
c. IBM System / 360
d. VAX-10

94) Which of the following terms is the most closely related to main memory?
a. Non volatile
b. Permanent
c. Control unit
d. Temporary

95) Which of the following is used for manufacturing chips?
a. Control bus
b. Control unit
c. Parity unit
d. Semiconductor

96) To locate a data item for storage is
a. Field
b. Feed
c. Database
d. Fetch

97) A directly accessible appointment calendar is feature of a … resident package a. CPU
b. Memory
c. Buffer
d. ALU

98) The term gigabyte refers to
a. 1024 bytes
b. 1024 kilobytes
c. 1024 megabytes
d. 1024 gigabyte

99) A/n …. Device is any device that provides information, which is sent to the CPU **a. Input**
b. Output
c. CPU
d. Memory

100) Current SIMMs have either … or … connectors (pins)
a. 9 or 32
b. 30 or 70
c. 28 or 72
d. 30 or 72

101) Which is the brain of computer:
a. ALU
b. **CPU**
c. MU
d. None of these

102) Which technology using the microprocessor is fabricated on a single chip: a. POS
b. **MOS**
c. ALU

d. ABM

103) MOS stands for:

a. **Metal oxide semiconductor**

b. Memory oxide semiconductor

c. Metal oxide select

d. None of these

104) In which form CPU provide output:

a. Computer signals

b. **Digital signals**

c. Metal signals

d. None of these

105) The register section is related to_____ of the computer: a. Processing

b. ALU

c. **Main memory**

d. None of these

106) In Microprocessor one of the operands holds a special register called: a. Calculator

b. Dedicated

c. **Accumulator**

d. None of these

107) Which register is a temporary storage location:

a. general purpose register

b. dedicated register

c. **A and B**

d. none of these

108) PC stands for:

a. **Program counter**

b. Points counter

c. Paragraph counter

d. Paint counter

109) IR stands for:

a. Intel register

b. In counter register

c. Index register

d. **Instruction register**

110) SP stands for:

a. Status pointer

b. **Stack pointer**

c. a and b

d. None of these

111) The act of acquiring an instruction is referred as the____ the instruction: a. **Fetching**

b. Fetch cycle

c. Both a and b

d. None of these

112) How many bit of instruction on our simple computer consist of one____: a. 2-bit
b. 6-bit
c. **12-bit**
d. None of these

113) How many parts of single address computer instruction : a. 1
b. **2**
c. 3
d. 4

114) Single address computer instruction has two parts:
a. The operation code
b. The operand
c. **A and B**
d. None of these

115) LA stands for:
a. **Load accumulator**
b. Least accumulator
c. Last accumulator
d. None of these

116) Which are the flags of status register:
a. Over flow flag
b. Carry flag
c. Half carry flag
d. Zero flag
e. Interrupt flag
f. Negative flag
g. **All of these**

117) The carry is operand by:
a. C
b. D
c. S
d. O

118) The sign is operand by:
a. S
b. D
c. C
d. O

119) The zero is operand by:
a. Z
b. D
c. S
d. O

120) The overflow is operand by:

a. O

b. D

c. S

d. C

121) _____ Stores the instruction currently being executed:

a. **Instruction register**

b. Current register

c. Both a and b

d. None of these

122) In which register instruction is decoded prepared and ultimately executed:

a. **Instruction register**

b. Current register

c. Both a and b

d. None of these

123) The status register is also called the____:

a. Condition code register

b. Flag register

c. **A and B**

d. None of these

124) The area of memory with addresses near zero are called:

a. High memory

b. Mid memory

c. Memory

d. Low memory

125) The processor uses the stack to keep track of where the items are stored on it this by using the:

a. **Stack pointer register**

b. Queue pointer register

c. Both a & b

d. None of these

126) Stack words on:

a. LILO

b. **LIFO**

c. FIFO

d. None of these

127) Which is the basic stack operation:

a. PUSH

b. POP

c. **BOTH A and B**

d. None of these

128) SP stand for:

a. **Stack pointer**

b. Stack pop

c. Stack push
d. None of these

129) How many bit stored by status register:
a. **1 bit**
b. 4 bit
c. 6 bit
d. 8 bit

130) The 16 bit register is separated into groups of 4 bit where each groups is called:
a. BCD
b. **Nibble**
c. Half byte
d. None of these

131) A nibble can be represented in the from of:
a. Octal digit
b. Decimal
c. **Hexadecimal**
d. None of these

132) The left side of any binary number is called:
a. Least significant digit
b. **Most significant digit**
c. Medium significant digit
d. low significant digit

133) MSD stands for:
a. Least significant digit
b. **Most significant digit**
c. Medium significant digit
d. low significant digit

134) _____ a subsystem that transfer data between computer components inside a computer or between computer:
a. Chip
b. Register
c. Processor
d. **Bus**

135) The external system bus architecture is created using from _____ architecture:
a. Pascal
b. Dennis Ritchie
c. Charles Babbage
d. **Von Neumann**

136) Which bus carry addresses:
a. System bus
b. **Address bus**
c. Control bus
d. Data bus

137) A 16 bit address bus can generate___ addresses:

a. 32767
b. 25652
c. **65536**
d. none of these

138) CPU can read & write data by using :
a. Control bus
b. **Data bus**
c. Address bus
d. None of these

139) Which bus transfer singles from the CPU to external device and others that carry singles from external device to the CPU:
a. **Control bus**
b. Data bus
c. Address bus
d. None of these

140) When memory read or I/O read are active data is to the processor
: a. **Input**
b. Output
c. Processor
d. None of these

141) When memory write or I/O read are active data is from the processor: a. Input
b. **Output**
c. Processor
d. None of these

142) CS stands for:
a. Cable select
b. **Chip select**
c. Control select
d. Cable system

143) WE stands for:
a. **Write enable**
b. Wrote enable
c. Write envy
d. None of these

144) MAR stands for:
a. **Memory address register**
b. Memory address recode
c. Micro address register
d. None of these

145) MDR stands for:
a. **Memory data register**
b. Memory data recode
c. Micro data register

d. None of these

146) Which are the READ operation can in simple steps: a. Address
b. Data
c. Control
d. **All of these**

147) DMA stands for:
a. **Direct memory access**
b. Direct memory allocation
c. Data memory access
d. Data memory allocation

148) The ____ place the data from a register onto the data bus: a. **CPU**
b. ALU
c. Both A and B
d. None of these

149) The microcomputer system by using the ____device interface: a. Input
b. Output
c. **Both A and B**
d. None of these

150) The standard I/O is also called:
a. **Isolated I/O**
b. Parallel I/O
c. both a and b
d. none of these

151) The external device is connected to a pin called the _____ pin on the processor chip. a. **Interrupt**
b. Transfer
c. Both
d. None of these

152) Which interrupt has the highest priority?
a) INTR
b) TRAP
c) RST6.5
d) none of these

153) In 8085 name the 16 bit registers?
a) Stack pointer
b) Program counter
c) a & b
d) none of these

154) What are level Triggering interrupts?
a) INTR&TRAP
b) RST6.5&RST5.5
c) RST7.5&RST6.5

d) none of these

155) Which stack is used in 8085?

a) FIFO

b) LIFO

c) FILO

d) none of these

156) What is SIM?

a) Select Interrupt Mask

b) Sorting Interrupt Mask

c) Set Interrupt Mask.

d) none of these

157) RIM is used to check whether, _____

a) The write operation is done or not

b) The interrupt is Masked or not

c) a & b

d) none of these

158) In 8086, Example for Non maskable interrupts are

a) Trap b) RST6.5 c) INTR d) none of these

159) In 8086 microprocessor the following has the highest priority among all type interrupts.

a) NMI

b) DIV 0

c) TYPE 255

d) OVER FLOW

160) BIU STAND FOR:

a. **Bus interface unit**

b. Bess interface unit

c. A and B

d. None of these

161) EU STAND FOR:

a. **Execution unit**

b. Execute unit

c. Exchange unit

d. None of these

162) Which are the part of architecture of 8086: a. The bus interface unit

b. The execution unit

c. **Both A and B**

d. None of these

163) Which are the four categories of registers:

a. General- purpose register

b. Pointer or index registers

c. Segment registers

d. Other register

e. **All of these**

164) IP Stand for:

a. **Instruction pointer**
b. Instruction purpose
c. Instruction paints
d. None of these

165) CS Stand for:
a. **Code segment**
b. Coot segment
c. Cost segment
d. Counter segment

166) DS Stand for:
a. **Data segment**
b. Direct segment
c. Declare segment
d. Divide segment

167) Which are the segment:
a. CS: Code segment
b. DS: data segment
c. SS: Stack segment
d. ES:extra segment
e. **All of these**

168) The acculatator is 16 bit wide and is called: a. **AX**
b. AH
c. AL
d. DL

169) The upper 8 bit are called_____:
a. BH
b. BL
c. **AH**
d. CH

170) The lower 8 bit are called_____:
a. **AL**
b. CL
c. BL
d. DL

171) IP stand for:
a. Industry pointer
b. **Instruction pointer**
c. Index pointer
d. None of these

172) Which has great important in modular programming: a. **Stack segment**
b. Queue segment
c. Array segment

d. All of these

173) Which register containing the 8086/8088 flag:
a. **Status register**
b. Stack register
c. Flag register
d. Stand register

174) How many bits the instruction pointer is wide: a. **16 bit**
b. 32 bit
c. 64 bit
d. 128 bit

175) How many type of addressing in memory: a. Logical address
b. Physical address
c. **Both A and B**
d. None of these

176) The size of each segment in 8086 is:
a. **64 kb**
b. 24 kb
c. 50 kb
d. 16kb

177) The physical address of memory is :
a. **20 bit**
b. 16 bit
c. 32 bit
d. 64 bit

178) The _____ address of a memory is a 20 bit address for the 8086 microprocessor: a. **Physical**
b. Logical
c. Both
d. None of these

179) The pin configuration of 8086 is available in the_____:
a. **40 pin**
b. 50 pin
c. 30 pin
d. 20 pin

180) DIP stand for:
a. Deal inline package
b. **Dual inline package**
c. Direct inline package
d. Digital inline package

181) PA stand for:
a. Project address
b. **Physical address**
c. Pin address

d. Pointer address

182) SBA stand for:
a. Segment bus address
b. Segment bit address
c. **Segment base address**
d. Segment byte address

183) EA stand for:
a. **Effective address**
b. Electrical address
c. Effect address
d. None of these

184) BP stand for:
a. Bit pointer
b. **Base pointer**
c. Bus pointer
d. Byte pointer

185) DI stand for:
a. **Destination index**
b. Defect index
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d. Delete index

186) SI stand for:
a. Stand index
b. **Source index**
c. Segment index
d. Simple index

187) DS stand for:
a. **Default segment**
b. Defect segment
c. Delete segment
d. Definition segment

188) ALE stand for:
a. **Address latch enable**
b. Address light enable
c. Address lower enable
d. Address last enable [1]

189) AD stand for:
a. **Address data**
b. Address delete
c. Address date
d. Address deal

190) NMI stand for:
a. **Non mask able interrupt**
b. Non mistake interrupt

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[1] cwipedia.in

c. Both
d. None of these

191) PC stand for:
a. **program counter**
b. project counter
c. protect counter
d. planning counter

192) AH stand for:
a. **Accumulator high**
b. Address high
c. Appropriate high
d. Application high

193) AL stand for:
a. **Accumulator low**
b. Address low
c. Appropriate low
d. Application low

194) The offset of a particular segment varies from _____:
a. 000H to FFFH
b. **0000H to FFFFH**
c. 00H to FFH
d. 00000H to FFFFFH

195) _____ is usually the first level of memory access by the microprocessor: a. **Cache memory**
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196) which is the small amount of high- speed memory used to work directly with the microprocessor:
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b. Case
c. Cost
d. Coos

197) The cache usually gets its data from the_____ whenever the instruction or data is required by the CPU:
a. **Main memory**
b. Case memory
c. Cache memory
d. All of these

198) How many type of cache memory:
a. 1
b. 2
c. **3**
d. 4

199) Which is the type of cache memory:

a. Fully associative cache
b. Direct-mapped cache
c. Set-associative cache
d. **All of these**

200)) Which memory is used to holds the address of the data stored in the cache
: a. **Associative memory**
b. Case memory
c. Ordinary memory
d. None of these